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Double-Sided Wafer Alignment Techniques

by Timothy J. Mermagen
Bruce R. Geil

U.S. Army Laboratory Command
Harry Diamond Laboratories
Adelphi, MD 20783-1197

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Timothy J. Mermagen and Bruce R. Geil

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Harry Diamond Laboratories
2800 Powder Mill Road
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13. ABSTRACT *(Maximum 200 words)*

A project was undertaken by the Harry Diamond Laboratories to develop a double-sided wafer alignment technique by which special-purpose devices could be fabricated using in-house equipment.. The approach developed was inexpensive and did not require infrared alignment methods for viewing through the wafer. A double-sided alignment technique with two different accuracies was developed for use on an ordinary optical mask aligner. These methods were highly successful and are in active use today.

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1. Introduction

Front-to-back wafer alignment has been a problem for the semiconductor industry because of the cost and limited availability of the specialized equipment needed to easily perform this task. The user of an optical contact printer cannot see through the wafer to align the pattern on the front of the wafer to that on the back, as is possible with an infrared contact printer. In optical contact printing, therefore, problems with wafer rotation and displacement arise when the front and back patterns must be aligned. To solve these problems, a mask alignment technique has been designed in the Semiconductor Engineering and Materials Technology (SEMT) Facility of the Harry Diamond Laboratories (HDL). This technique allows the user to contact print quickly with a front-to-back alignment accuracy of better than 50 μm without the use of expensive through-the-wafer alignment equipment.

Two separate projects required accurately aligned photolithography on both sides of double-polished silicon wafers. The first project was fabrication of a chip for an in-house research program.[1] The second was fabrication of floating cantilever beams to be used as accelerometer switches.[2] The technique developed for aligning the patterns on the front and back of a wafer for these projects is described in this report.

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[1]*Judith McCullen, Robert B. Reams, and Jonathan M. Terrell,* ***Failure Analysis of Loaded SCI Primers,*** *Harry Diamond Laboratories, HDL-PR-91-3 (September 1991).*

[2]*Theodore V. Blomquist and Timothy J. Mermagen,* ***Fabrication Process for Cantilever Beam Type Micromechanical Switch,*** *in preparation.*

2. Alignment Technique

The alignment technique developed at HDL was devised for use with a one-to-one (no reduction) mask aligner. This technique was used with two alignment accuracies for the projects mentioned above; variations of this technique can also be used to pattern integrated circuits.

2.1 Lower Alignment Accuracy Technique

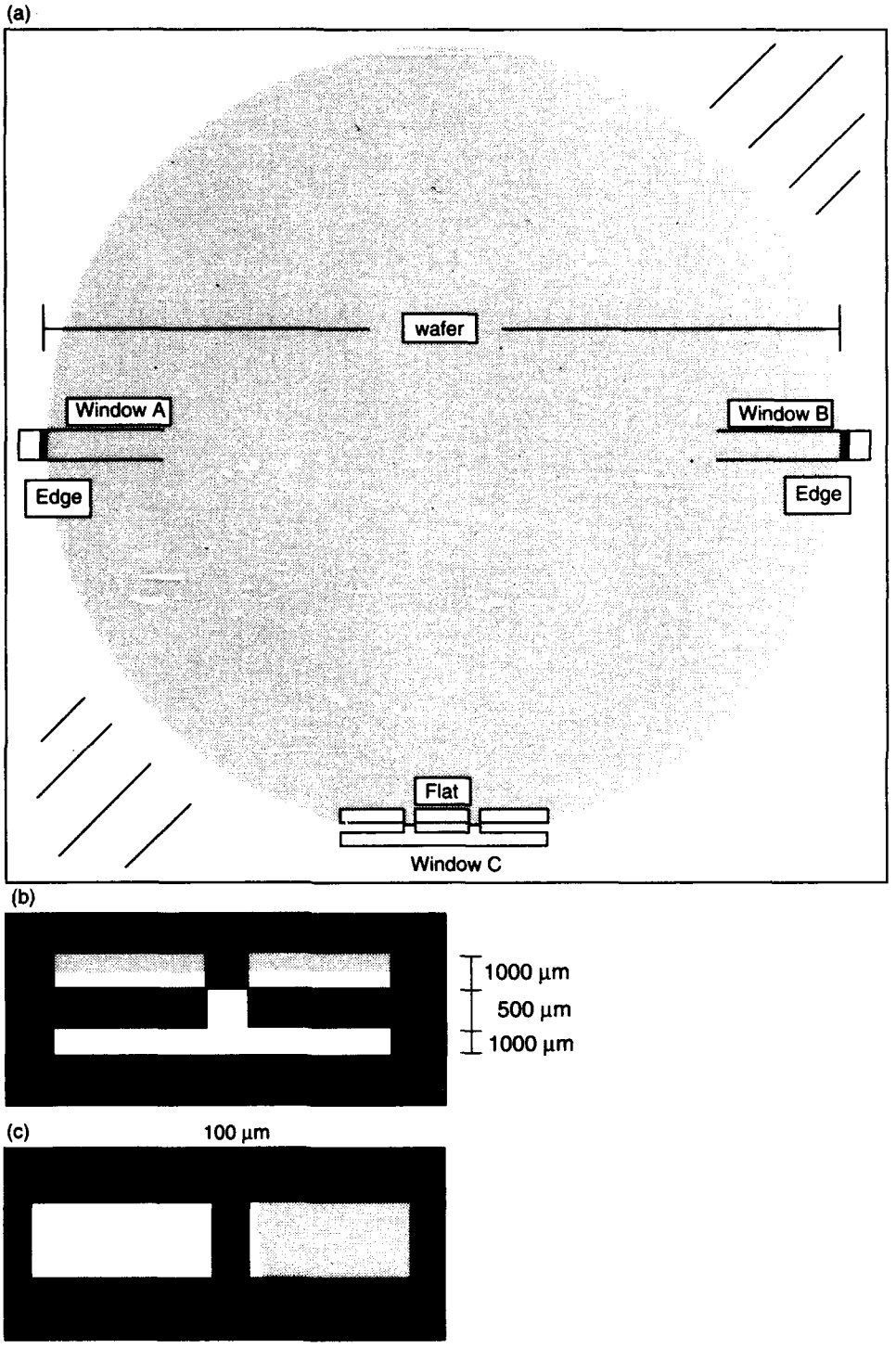
In the lower accuracy technique, the sides and flat of the wafer are used for aligning a mask to a wafer on a one-to-one mask aligner; figure 1a shows the mask used for this alignment accuracy. The mask consists of the first-level pattern with inter-level alignment marks (for same-side mask alignment) and the wafer edge windows. A *window* is an area where the chrome surface of a photomask has been removed, leaving the glass substrate uncovered. This allows for through-the-mask viewing.

Window C is used to align the flat of the wafer (fig. 1b and 2a). The user aligns the flat to the 500-μm bar separating the two 1000-μm-wide alignment windows. The lower part of window C is used to help find the flat of the wafer when higher magnifications are used. The user then aligns the flat as well as possible. When the back side of the wafer is imaged, this flat alignment will correct for rotational problems and correct for y-axis shift.

Once the flat of the wafer is aligned, the next step is the alignment of the wafer edge. Windows A and B are used for aligning the right or left edge of the wafer. These large windows contain a 100-μm bar that is used for aligning the wafer edge (see fig. 1c and 2b). Whichever edge/window is selected for alignment, the opposite edge/window must be used when the back of the wafer is aligned. This allows the die spacing to originate from the same side of the wafer, so that the front and back patterns on the wafer are aligned.

This alignment scheme produces better than 50-μm accuracy. This technique was successfully used to produce over 4000 test chips for an in-house research program (see fig. 3).

Figure 1. Lower accuracy alignment technique (a) mask, (b) flat alignment window, and (c) edge alignment window.



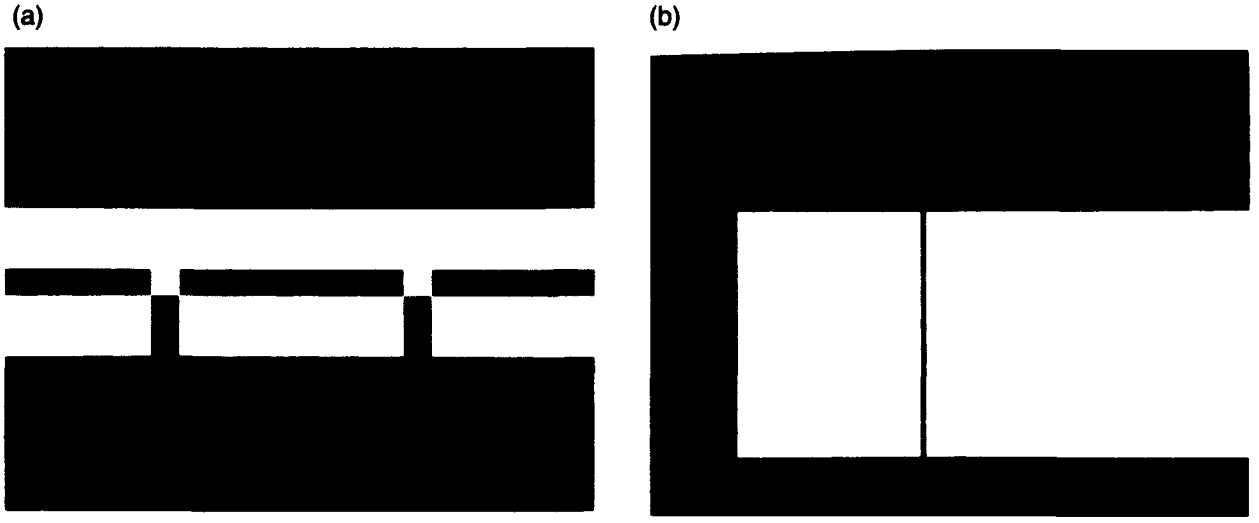


Figure 2. Alignment windows: (a) flat and (b) edge alignment window with 100-μm bar.

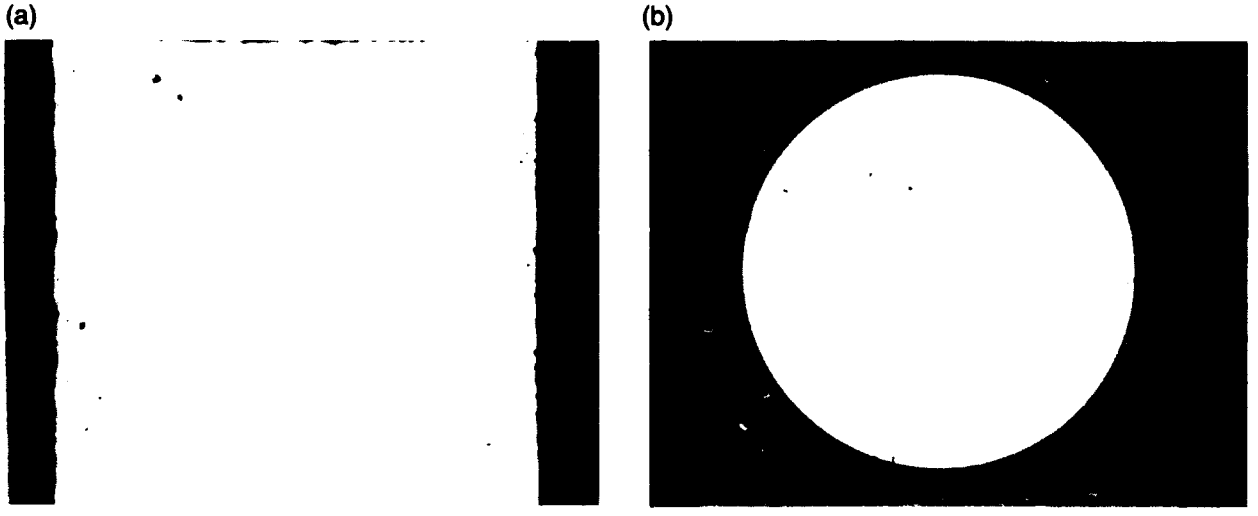


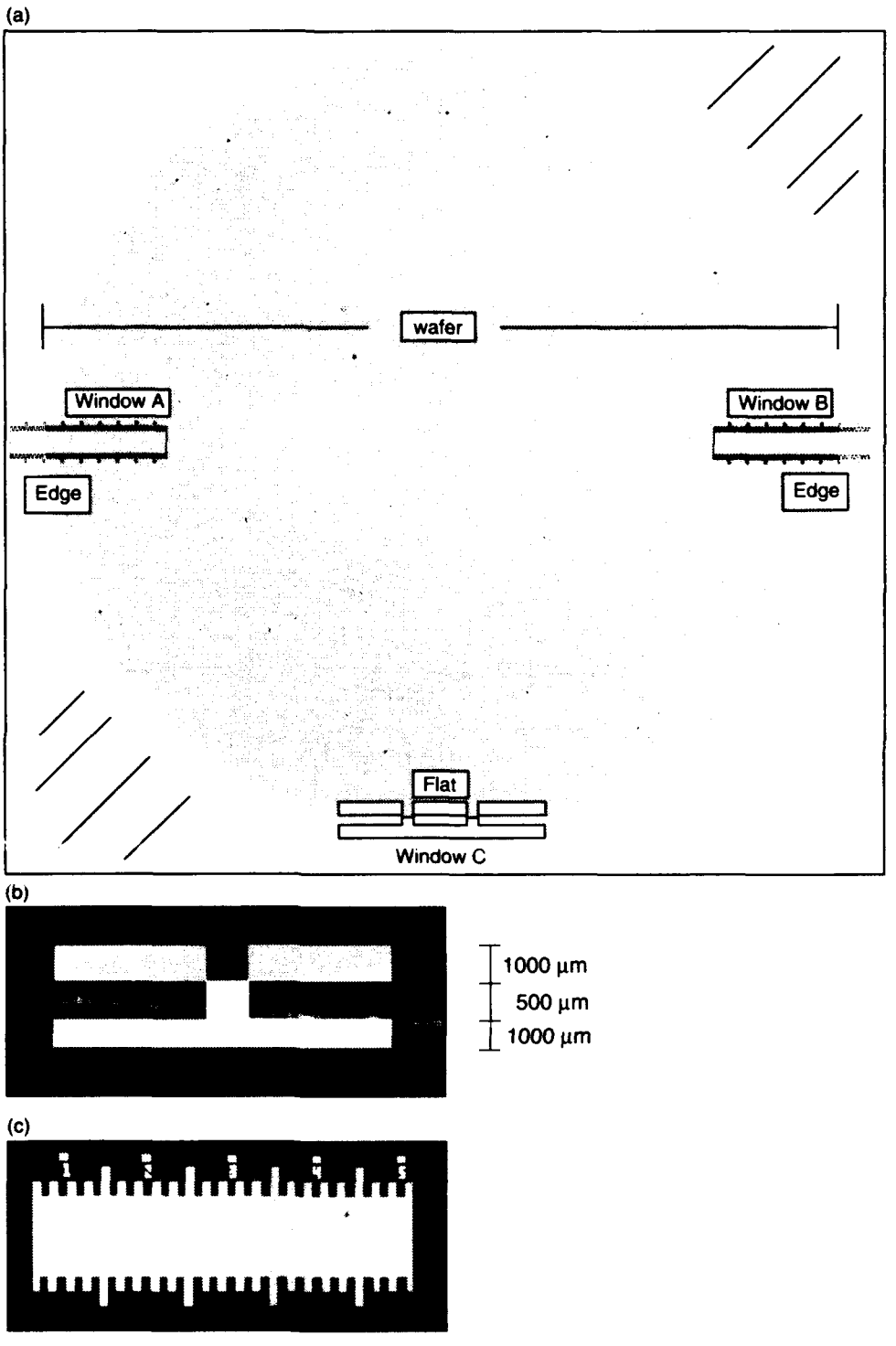
Figure 3. Semiconductor ignitor chip: (a) front view and (b) back view.

2.2 Higher Alignment Accuracy Technique

The second alignment technique also uses the sides and flat of the wafer to align a mask set on a one-to-one mask aligner, but it provides much higher accuracy (25 μm) and is much more difficult and time consuming to use. This mask alignment technique was used in the fabrication of floating cantilever beams.

The mask used in this technique has similar alignment windows to the previously described alignment mask. Window C is used in the same manner as in the first alignment mask: for aligning the flat of the wafer to correct for image rotation; it also aligns the wafer in the *y*-axis (fig. 4a and 4b). Again, once the flat is aligned, the wafer edge alignment is performed.

Figure 4. Higher accuracy alignment technique: (a) mask, (b) flat alignment window, and (c) edge alignment window.



Windows A and B are used similarly to the way they are used in the first alignment technique, but in the higher accuracy technique they have an alignment ruler consisting of 5-μm lines on 10-μm centers (fig. 4c). As shown in figure 5, the ruler uses numbers and symbols (instead of two-digit numbers) to identify the bars for easy alignment (symbols were used rather than numerals to cut down on the number of images used, thus saving mask imaging time). As in the first alignment technique, one side of the wafer is aligned to a particular number and demarcation symbol. When the back side of the wafer is imaged, the opposite edge/window must be used to align the die; this allows the die spacing to originate from the same side of the wafer, so that the front and back patterns on the wafer are aligned.

This alignment scheme produces better than 25-μm accuracy from front to back of the wafer. Several hundred cantilever accelerometers were produced using this method (see fig. 6).

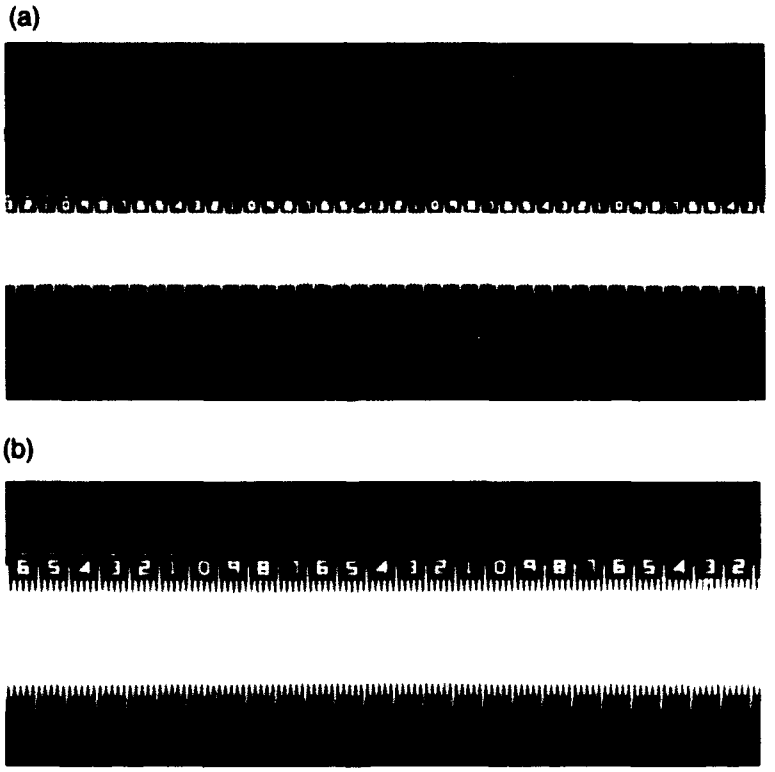


Figure 5. Edge alignment window with symbol bar.

(a)

(b)

Figure 6. Scanning electron microscope photographs of cantilever beam accelerometer: (a) top view and (b) side view.

3. Results

The results obtained with these alignment techniques have been very promising. With these techniques, we have produced over 4000 chips in support of the in-house research program and over 200 cantilever beam accelerometers. We have achieved a front-to-back wafer alignment accuracy of better than 50 μm with the lower accuracy technique and 25 μm with the higher accuracy technique on an ordinary optical contact printer.

4. Conclusions

The alignment techniques discussed here were very successful in aligning patterns on the top and back of a wafer and were used in producing chips and cantilever beam accelerometers. These techniques allow an inexpensive optical mask aligner system to be used to achieve much the same results as a more expensive infrared mask aligner.

Acknowledgements

The authors wish to acknowledge the assistance of two people in the work reported herein: Bernard Rod, HDL, for his work on the cantilever beam accelerometers; and Judith McCullen, HDL, for her untiring feedback on the alignment strategies and optical tooling of the in-house test chips and the cantilever beam accelerometer chips. The authors would also want to thank the rest of the Semiconductor Engineering and Materials Technology group for their support in this program.

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